IDEC Chip Design Contest

A 90.5%-Efficiency 28.7μV_{RMS}-Noise Bipolar-Output High- Step-Up SC DC-DC Converter with Energy-Recycled Regulation and Post-Filtering for ±15V TFT-Based LAE Sensors

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❖ Abstract

- **In this paper, a ±15V bipolar-output high step-up SC DC-DC converter with energy-recycled regulation Presented. An energy-recycled fine regulation scheme in step-up SC converter. It accurately controls the dropout voltage of post-regulator to be minimal. Such improvements were achieved without increasing the complexity (cost) overhead or the power loss in the SC circuit. Also, the proposed load-current reused (LCR) post-regulator offers high suppression of switching ripple and noise wile maintaining a voltage efficiency of 98.7%. The chip fabricated in 180-nmBCD offers 28.7μV_{RMS} output noise and a total peak efficiency of 90.5%.**

❖ Proposed

- **Energy-Recycled Optimal Dropout(V_{DO}) Control (EROC):** Minimize the dropout voltage of the post-regulator
- **Voltage/Current-Hybrid (VIH) Post Regulation:** High PSR & High efficiency
- **Load-Current-Reused (LCR) Voltage Regulation:** Low circuit noise

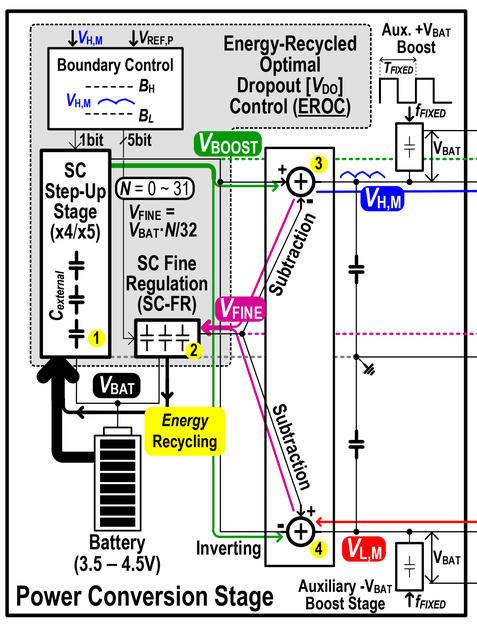


Fig. 1. Proposed DC-DC converter with energy-recycled regulation

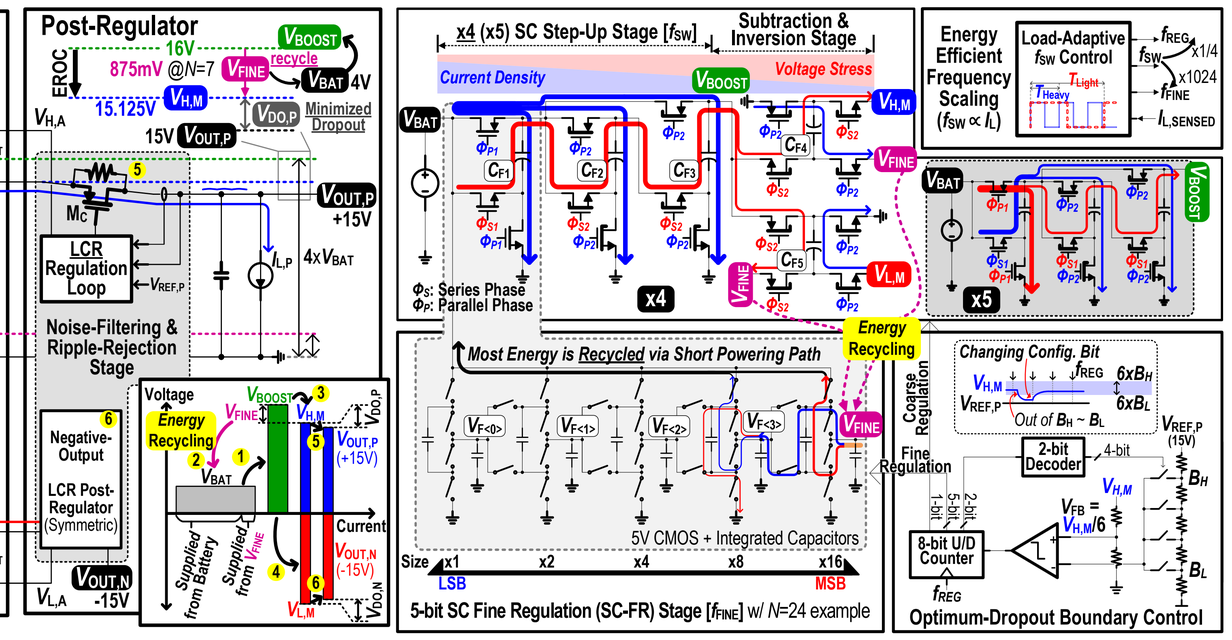
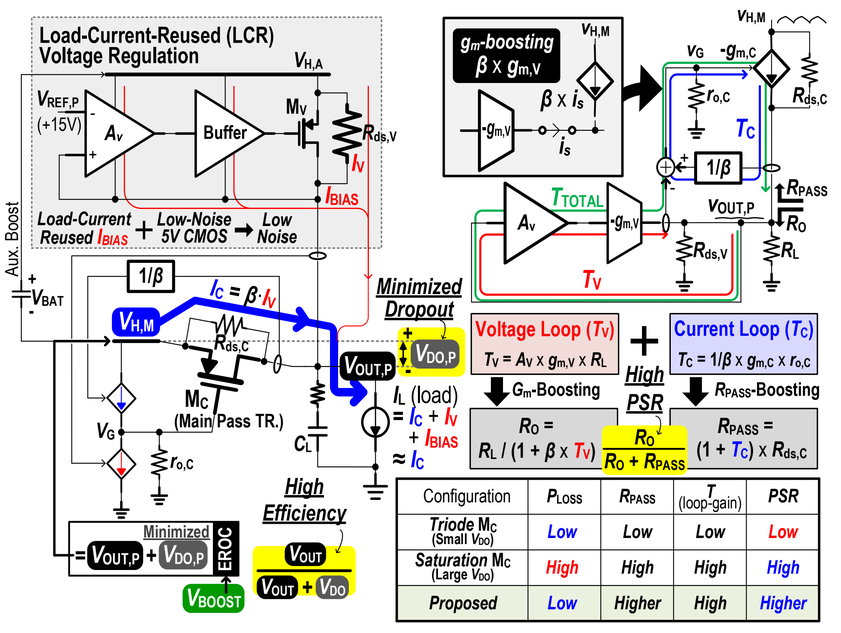


Fig. 2. Detailed implementation of the SC power conversion stage



Configuration	P_{LOSS}	R_{PASS}	$T_{(loop\text{-}gain)}$	PSR
Triode M_C (Small V_{DO})	Low	Low	Low	Low
Saturation M_C (Large V_{DO})	High	High	High	High
Proposed	Low	Higher	High	Higher

Fig. 3. Proposed concept of load-current-reused (LCR) post-regulator

❖ Measurement Results

- **Maximum 90.5% conversion efficiency including power conversion stage and post-filtering stage**
- **Under 28.7μV_{RMS} noise integrated from 100Hz to 500kHz at 20mA load current**

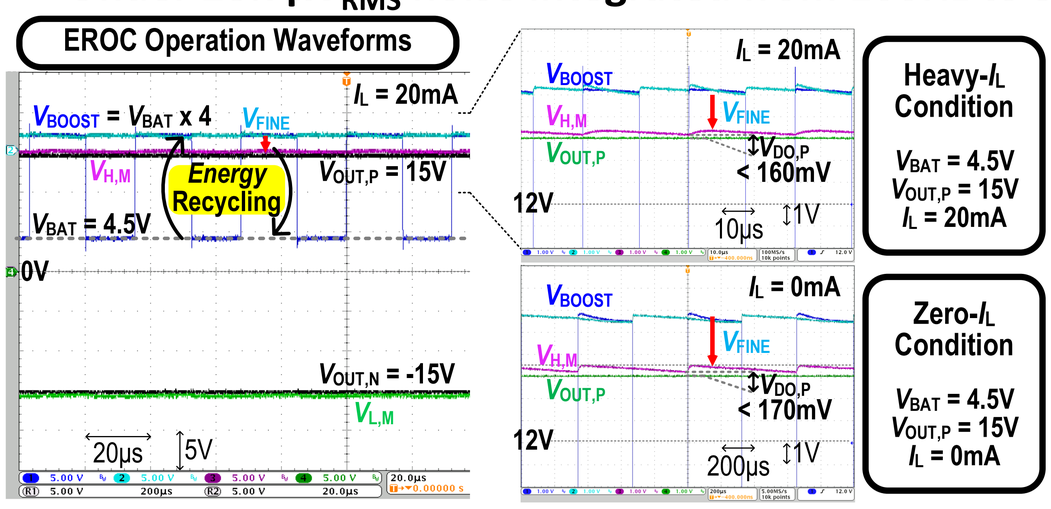


Fig. 4. Measured steady-state waveforms

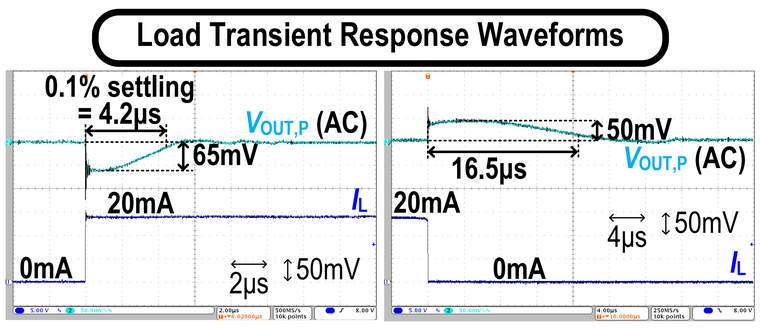


Fig. 5. Measured load transient response waveforms

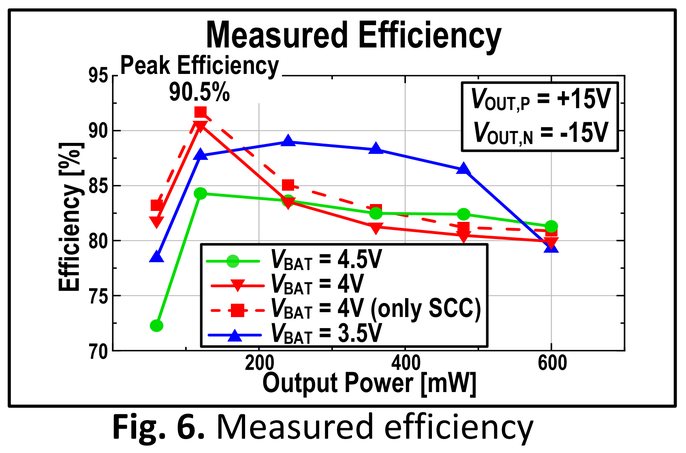


Fig. 6. Measured efficiency

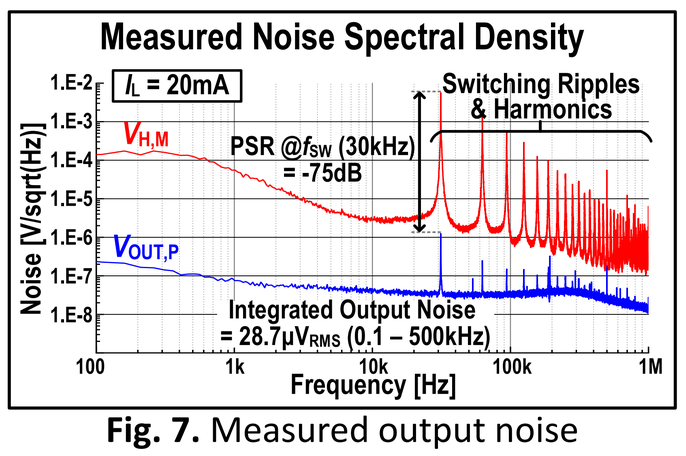


Fig. 7. Measured output noise

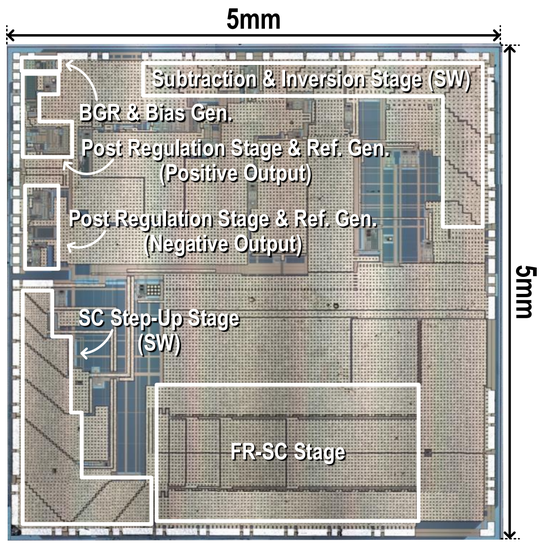


Fig. 8. Die Micrograph

❖ Conclusion

- **The proposed DC-DC converter achieved high efficiency in the wide input voltage and load current range. Due to the role division of post-filtering stage, it shows low noise performance without efficiency degradation.**

❖ Acknowledgement

- **The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.**

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